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Stencil lithography for bridging MEMS and NEMS

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ABSTRACT

The damage inflicted to silicon nanowires (Si NWs) during the HF vapor etch release poses a challenge to the monolithic integration of Si NWs with higher-order structures, such as microelectromechanical systems (MEMS). This paper reports the development of a stencil lithography-based protection technology that protects Si NWs during prolonged HF vapor release and enables their MEMS integration. Besides, a simplified fabrication flow for the stencil is presented offering ease of patterning of backside features on the nitride membrane. The entire process on Si NW can be performed in a resistless manner. HF vapor etch damage to the Si NWs is characterized, followed by the calibration of the proposed technology steps for Si NW protection. The stencil is fabricated and the developed technology is applied on a Si NW-based multiscale device architecture to protectively coat Si NWs in a localized manner. Protection of Si NW under a prolonged (>3 h) HF vapor etch process has been achieved. Moreover, selective removal of the protection layer around Si NW is demonstrated at the end of the process. The proposed technology also offers access to localized surface modifications on a multiscale device architecture for biological or chemical sensing applications.

1. Introduction

Microelectromechanical systems (MEMS) technology-based sensors constitute a multi-billion-dollar market with market revenue projected to reach 16.85 billion, driven by their diverse applications in the automobile, aerospace, consumer electronics, and biomedical sectors [1]. Accompanied by the miniaturization of electronics, MEMS manufacturers are tasked with meeting the increasing demand for ultra-low power, high-performance, and compact sensors. Besides improving the performance of the existing sensors to fulfill market expectations, cost reduction is also necessary for sustainable market growth. Therefore, a cost reduction of 10 to 12% is expected each year to sustain the market growth while exploring new application areas for MEMS sensors [2]. Miniaturization of the sensors appears to have the potential to achieve these goals. Modern MEMS sensors typically employ piezoresistive, piezoelectric, or capacitive transduction schemes for input sensing. However, piezoelectric- and capacitive-based MEMS transduction technologies would suffer from miniaturization, as their sensing performance drops with the miniaturization of the transducer. Meanwhile, resulting from miniaturization, silicon nanowire (Si NW)-based piezoresistive transduction scheme results in a substantial reduction of sensor size, coupled with mechanical amplification, large piezoresistive coefficient, high signal-to-noise ratio, and immunity to the electromagnetic interference of transduction element [3].

A generic architecture for Si NW-based sensors usually involves a piezoresistive Si NW transduction element integrated with a MEMS shuttle. MEMS shuttle converts the external input of, for example, inertial force to minute deflections, while the transduction element is employed as a sensitive structure to measure the induced deflection. Efforts have been intensified over the past decade for the monolithic fabrication of Si NWs with MEMS shuttles for such inertial sensors [3]. In this regard, monolithic fabrication of Si NW-based accelerometers [4,5], gyroscopes [6], as well as pressure sensors [7,8], and magnetometers [9] have been successfully demonstrated, utilizing thick and thin silicon on

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insulator (SOI)-based fabrication technologies [4,10]. However, the monolithic fabrication for these sensors is usually challenging due to an order of magnitude geometrical size difference between the NW and shuttle. One of the leading challenges is releasing the MEMS shuttle via etching the underneath buried oxide (BOX) layer through hydrogen fluoride (HF) vapor etch.

Despite the high value of etch selectivity of the BOX layer over the silicon layer, HF vapor etching potentially does considerable damage to the Si NWs due to the miniaturized dimensions. Therefore, the situation is usually circumvented by avoiding prolonged etching time needed for the shuttle release. The goal is generally achieved by placing the through-shuttle etch holes in very close proximity onto the shuttle geometry to reduce the characteristic dimension for HF vapor etch. However, through this approach, the geometrical design of the shuttle faces constraints as it becomes dependent on the geometrical dimensions of the Si NW.

This work reports a new technology based on stencil lithography to protect the Si NW during the HF vapor etch process for shuttle release. Stencil lithography is a resistless, high-resolution patterning technique previously used to pattern metallic NWs, nanodots, and for dry etching [11]. In this study a protective layer around NW is deposited to avoid damage to NW during the release process caused by HF vapor etch. Moreover, selective removal of the protective coating around the Si NW at the end of the process is demonstrated.

It is found that the proposed stencil lithography-based technology potentially mitigates challenges towards monolithically integrating Si NWs with higher-order sensing structures while enabling both shuttle and Si NW geometrical design independently.

2. Materials and methods

2.1. Materials

All of the procured chemicals were utilized without any further treatment. Photoresist AZ5214 (Microchemicals), KOH (technic, 44%), acetone (Technic), isopropyl alcohol (Technic), hydrofluoric acid (Technic, 50%), parylene-C pellets (plasma parylene systems), chromium target (Kurt J. Lesker, 99.95%), gold target (Kurt J. Lesker, 99.99%), gold etchant (Sigma Aldrich), and chromium etchant (Technic) were utilized as a part of the fabrication process flow for technology development. The deionized (DI) water was used during the fabrication to wash samples.

2.2. HF vapor etch damage characterization to Si NW

Fig. 1(a) shows a micrograph of Si NW-based multiscale device architecture fabricated via thick SOI-based fabrication technology [10,12]. An unreleased MEMS shuttle is anchored to the substrate through an order of magnitude smaller Si NW-based transduction element. The inset shows a tilted view of the Si NW bridging shuttle and anchors. With the device currently unreleased, having a BOX layer underneath the MEMS shuttle, HF vapor etching is required to release the thick shuttle. However, despite its high selectivity towards Si, HF vapor can significantly damage the Si NW due to its thin geometrical dimensions. Protection around Si NW during the release process can prevent damage to NW from HF vapor etching.

For the sensor presented in Fig. 1(a), HF vapor etch (Idonus VPE 150) is conducted to complete the final fabrication step and release the shuttle by removing the underneath BOX layer. First of all, a complete calibration for etch time required for shuttle release was carried out, which resulted in 3 h of etch time required for shuttle release. The shuttle is pushed manually through the needles for visual inspection of release. Meanwhile, throughout the HF vapor etch process, the electrical response of Si NW is monitored via probe I-V measurement (Agilent technologies B1500A) along with accompanying scanning electron microscope (SEM) images. Fig. 1(b) shows the state of NW throughout the HF etch intervals until the complete release of the shuttle. Before HF vapor etch, the electrical response of NW shows a linear voltage-current relation with a resistance of around 2.2 kΩ. The electrical response of Si NW is found to suffer degradation after about 1 h of HF vapor etch. The degradation is traced back to geometrical damage to Si NW during the release process caused by HF vapor. Three hours into the etch process until the complete release of the shuttle, the electrical response of Si NW vanishes, with an accompanied micrograph depicting total damage to Si

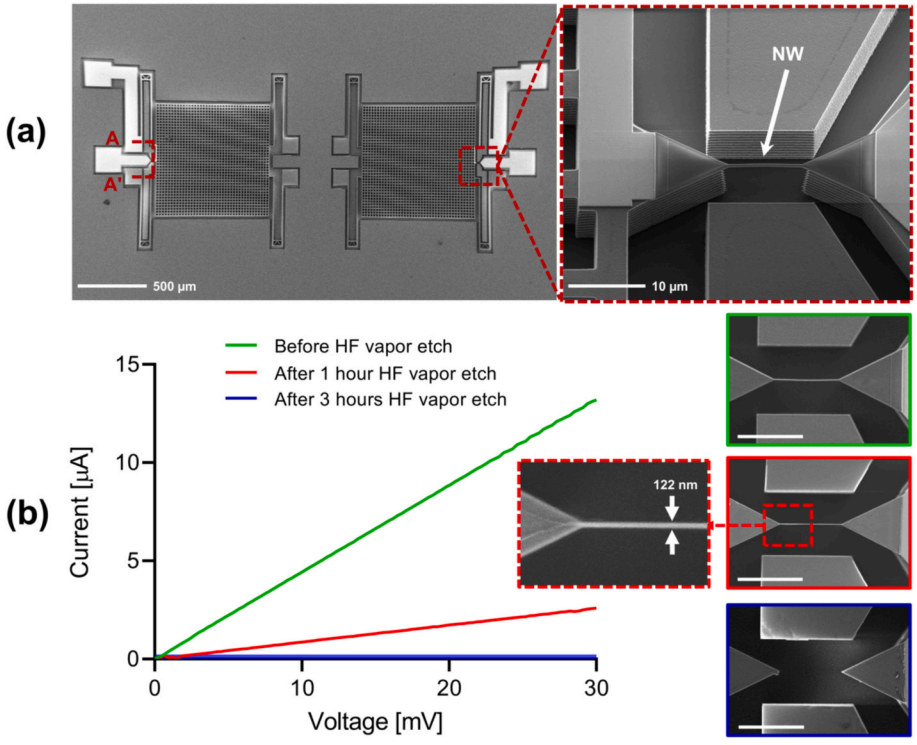


Fig. 1. (a) A Si NW-based piezoresistive sensor with differential pair of Si NW transduction elements fabricated through thick SOI-based fabrication technology, the inset shows the transduction element bridging the gap between the MEMS shuttle and the substrate anchor. The sensor is currently unreleased with the BOX layer underneath the MEMS structure. (b) Release of the sensor via etching the BOX layer through HF vapor etch. Si NW is fully damaged until the shuttle is completely released, as seen from probe I-V measurements and SEM micrograph. (The scale bars are 10 µm.)

NW. In the conventional approach, damage to the Si NW is minimized by shortening the release time duration, which, in turn, is achieved by placing multiple etch holes in very close proximity on the shuttle surface to provide easy access for HF vapors underneath BOX. However, this approach results in the design of the shuttle becoming dependent on Si NW dimensions as far as the release process is concerned. This practice limits the aim of enabling independent geometrical integration of Si NW in a multiscale device architecture via a monolithic fashion.

2.3. Stencil lithography-based protection technology

We design a stencil lithography-based protection technology for Si NW. Fig. 2(a) shows the proposed fabrication flow, depicted through section AA' of the Si NW-based sensor in Fig. 1. The process step (i) starts with an unreleased sensor chip containing Si NW transduction element. In the second step, (ii), a thin parylene-C layer is coated in a conformal manner all around the sensor, followed by selective deposition of a protective metal layer through physical vapor deposition (PVD) around the Si NW via stencil lithography in step (iii). Later step (iv) involves Oxygen (O_2) plasma reactive ion etching (RIE) to remove parylene-C from horizontal surfaces after the stencil lithography. Removal of parylene-C enables HF vapors access underneath BOX in the subsequent release step. The final step (v) involves releasing the shuttle via HF vapor etching. Here, the protective metal around Si NW protects it from damage caused by HF vapors. For some applications, an optional step involving etch of protective coating and parylene-C can also be carried out.

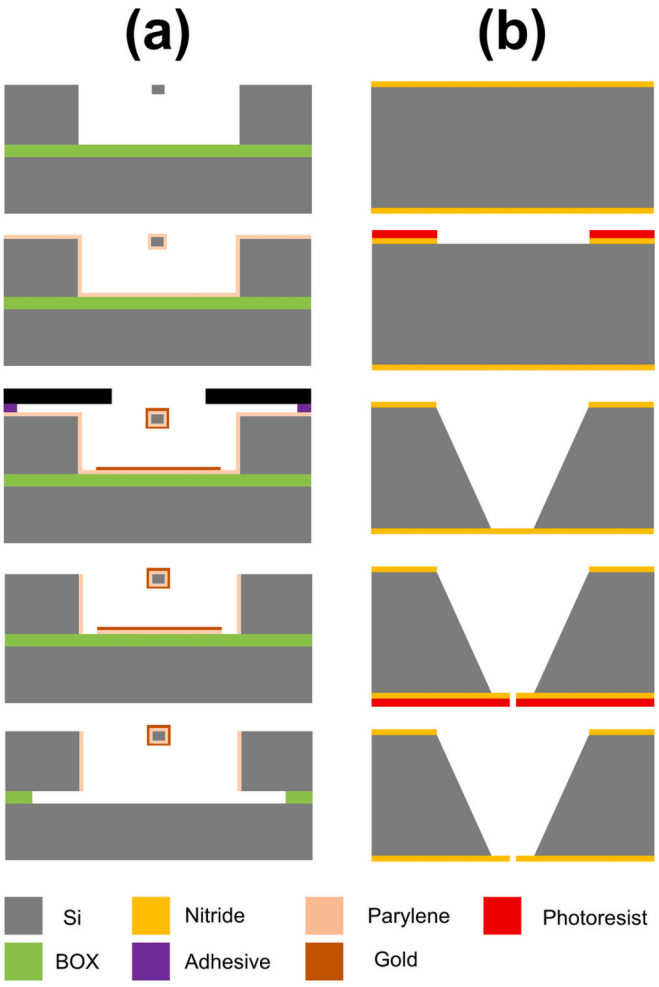


Fig. 2. (a) Proposed flow of stencil lithography-based protection technology for Si NWs during HF vapor etching. i) an unreleased sensor, ii) parylene-C conformal coating, iii) alignment of the Si NW-based sensor with the stencil and stencil lithography, iv) RIE of parylene-C from horizontal surfaces, v) release via HF vapor etch. (b) Stencil fabrication process flow. i) plasma enhanced chemical vapor deposition (PECVD) of Si nitride on double-side polished Si wafer, ii) photolithography of AZ5214 and patterning of nitride, iii) anisotropic KOH wet etching, iv) backside photolithography of AZ5214 and nitride patterning for opening stencil hole, v) photoresist removal and cleaning of the stencil.

For the stencil lithography step in the fabrication process flow, Fig. 2 (a), the stencil comprises a hole inside a Silicon nitride membrane coated on a Si wafer. Before stencil lithography, alignment is carried out between the stencil and sensor, and both are joined via a double-sided UV tape. After stencil lithography, flood UV exposure is carried out to remove the stencil from the sensor.

Fig. 2(b) shows the fabrication process flow for the stencil. In the first step, (i), silicon nitride is coated on both sides of a double-sided polished wafer, followed by patterning via dry etching in step (ii). Wet etching of Si is conducted via KOH in the subsequent process (iii), where Si nitride act as a masking layer. Later, (iv), backside patterning of the nitride is performed to create a hole that would serve as a stencil hole in the stencil lithography. The last step, (v), involves cleaning of the stencil to remove the residuals.

Conventional approaches reported in the literature for the stencil fabrication [13–17] involve alignment of the features patterned for KOH-etch window at the front side with a stencil hole patterned at the backside of the substrate, before performing KOH wet etch for Si. This alignment can be performed using front and backside alignment cameras of the lithography equipment; however, it needs sophisticated and expensive equipment. On the other hand, proposed stencil fabrication process offers a simplified approach for the alignment of the KOH-etch window and stencil hole on the substrate without the need for sophisticated equipment having a backside alignment camera. After the KOH etch in proposed process, Fig. 2(b), the hole created into Si substrate is visible on the backside due to the transparency of light through the thin nitride membrane. Hence, this hole itself is used as an alignment mark when patterning is performed to create the stencil hole into the nitride membrane. So, equipment with a backside camera for alignment purposes is not required. Moreover, with this two-step approach for separate patterning of KOH etch window and the stencil hole, since stencil patterning is performed after KOH etch so this makes stencil hole size independent of slight variation in KOH window size caused by KOH over-etch due to time. Besides, presented fabrication process flow approach in this paper also offers independent adjustment of the stencil hole size, as well as KOH window size via adjustment of the KOH etch duration.

2.4. Calibration

A complete calibration of all process steps was carried out as part of technology development, Fig. 2(a). 200 nm thin conformal layer of parylene-C was coated via parylene coater (PPS Labcoater Series 100). For the stencil lithography step, Fig. 2(b), a double-side polished Si wafer is coated on both sides with 100 nm Si nitride via PECVD (SENTECH SI 500D). Photoresist AZ5214 is coated and patterned on one side with maskless lithography (Heidelberg MLA 100), and RIE (SENTECH SI 500) is performed to pattern the nitride layer. Later, the photoresist is removed, and wet etching of Si is performed for 40 h in a bath containing a KOH diluted to 22% through DI water. A minute amount of IPA is added to reduce the Si etch roughness [18]. After the etch completion, AZ5214 is coated on the backside of the wafer, and the hole is patterned onto the photoresist after lithography alignment. The thin nitride and AZ5214 on top of it are transparent to the light, so the proposed stencil fabrication process approach offers easy alignment as part of double-side lithography. The size of the patterned hole on the backside determines the opening for selective deposition during the stencil lithography step in Fig. 2(a). RIE of nitride after photoresist patterning opens the hole

inside nitride on the backside. The photoresist is removed, and the wafer is cleaned with Acetone, IPA, and DI water and dried using dry nitrogen.

The stencil and the Si NW-based sensor are aligned for the PVD coating of metal as part of stencil lithography. Fig. 3 shows the setup utilized for the alignment, consisting of a set of in-plane stages that enable four degrees of freedom controlled by motorized actuators and a manual stage. Rotation of the sensor is possible through a manual rotation stage mounted on top of linear stages. The stencil is mounted on a stencil holder. At the same time, two degrees of freedom motion in the vertical axis is achieved through the movement of the objective and motorized actuator-controlled stage (Newport M-562). Precise alignment of the stencil with the sensor is achieved through motorized actuators. The stencil holder and the XYZ stage are commonly attached to a manual XY stage (Thorlabs) through a base plate. As more than one alignment mark is needed for translational and rotational alignment between the stencil and sensor, there are two alignment marks on the stencil to align with structures on the sensor. However, since the microscope objective is fixed and can only move on the vertical axis, the manual XY stage is used to move the whole setup housing stencil and sensor for checking to match of multiple alignment marks with sensor structures for rotational and translational alignment. The whole setup is mounted via manual XY stage on a vibration-free table to eliminate any misalignment caused by vibration during stencil-sensor contact. A 90 μm-thick double-sided UV tape (HUV-D7125-30P) is attached to the empty portion of the sensor, and the stencil is attached firmly to the sensor after alignment between the stencil and the sensor.

After alignment and attaching the stencil with the sensor, PVD equipment (K.J Lesker) with minimized target-stencil distance is chosen to coat a 100 nm thick protective layer around Si NW. Later, the stencil and sensor are de-attached via UV exposure (UVitron Intelliray 600) to the double-sided UV tape. As part of the calibration of the remaining process step, RIE of parylene-C is performed to remove it from horizontal surfaces, which is followed by HF vapor etching of the sensor to release the shuttle.

3. Results and discussion

Selective deposition via developed stencil lithography-based technology was carried out on Si NW-based multiscale device architecture, and shuttle release was performed by subjecting the sample to HF vapor etching. Micrographs of the sensor throughout the release process are obtained to monitor and analyze the condition of Si NW. Two sets of samples are chosen to depict the effectiveness of protection offered by the deposited metal via stencil lithography. Fig. 4(a) shows the micrographs of sample 1 obtained throughout the different stages of the developed technology. Si NW from an unreleased chip is subjected to stencil lithography, and two hours of HF vapor etch was performed on the sample, with a one-hour interval. The micrograph obtained after two hours of HF vapor etch reveals no damage to the Si NW.

Besides the etching with intervals, a second sample was prepared to depict the effectiveness of coated thickness of protective coating via stencil lithography against prolonged HF vapor etch time. The sensor was subjected to process steps of developed technology, Fig. 4(b), and three hours of HF vapor etch was performed in one step. The micrograph obtained after prolonged HF vapor etch reveals no damage to the Si NW, with no visual damage to the protective coating.

It is important to note that a minimum gap is desired between the stencil and sensor during the PVD process to minimize metal diffusion by preventing the coating of the area away from the region on the sensor exposed through the stencil hole. Meanwhile, the size of the stencil hole is chosen such that the deposition of metal occurs through the stencil hole onto Si NW during the PVD process. Material deposition through the stencil hole depends on stencil hole size, the gap between the stencil and NW sensor, and the stencil distance from the PVD target. For presented work, with the gap fixed at 90 μm between the stencil and NW-based sensor, the stencil distance from the PVD target is crucial in enabling deposition onto the sensor through the stencil hole.

Apart from the criteria mentioned above, deposition of protective metal via PVD all around the Si NW is the key for successful vapor HF damage protection. As directional PVD techniques, such as evaporation, would coat NW sidewalls partially and the bottom surface minimally, vapor HF can still damage the Si NW due to the isotropic nature of the etch. On the contrary, sputtering entails the potential for conformal coating on all NW surfaces. To check the state of sputtered protective coating, a NW cross-section is obtained through focused ion beam (FIB) milling after stencil lithography (Fig. 5(a-c)). Micrographs verify that Si NW is encapsulated within a dark parylene layer which is conformally buried underneath the protective metal. Energy dispersive X-ray spectroscopy (EDS) line spectra of the cross section in Fig. 5(d-e) corroborate further the presence of protective metal on all sides of the Si NW.

For some applications requiring the removal of protective coating at the end of successful release process, the stencil lithography-based protection flow presented in Fig. 2(a) can be modified by the etching of metal and parylene following the vapor HF release. For presented

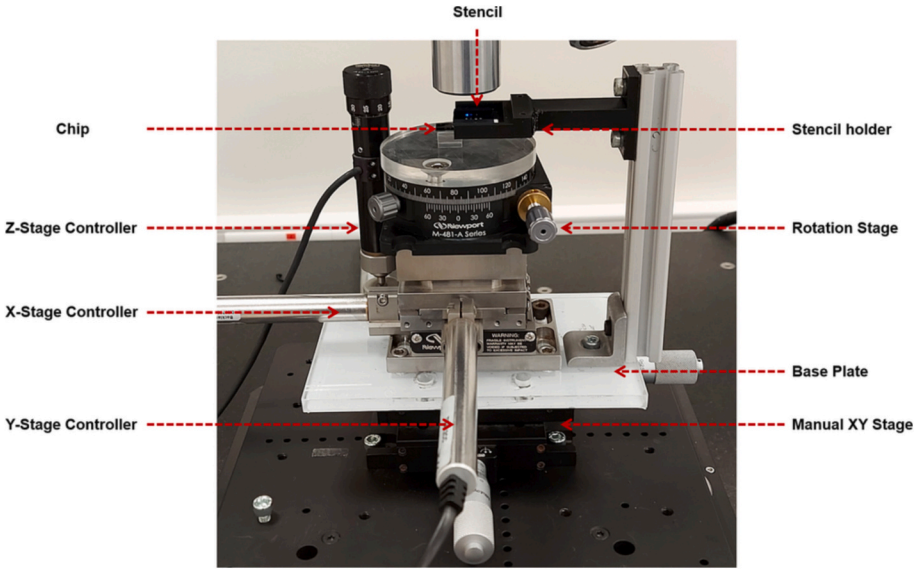


Fig. 3. The alignment setup utilized during the alignment between the hole on the stencil and NW on the Si NW-based sensor.

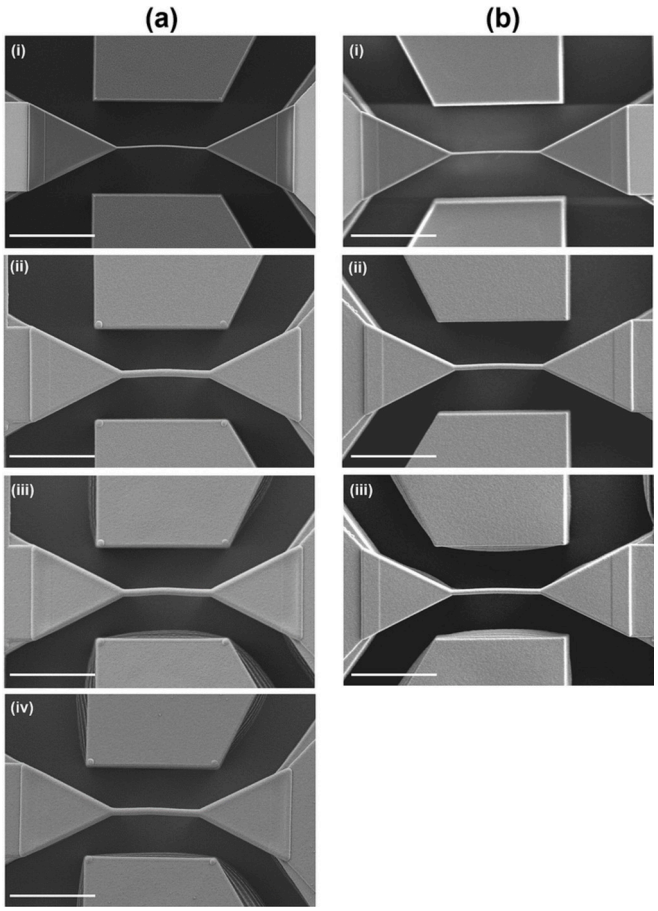


Fig. 4. Implementation of developed stencil lithography-based protection technology on Si NW-based sensors subjected to different HF vapor etch durations. Sample 1 is subjected to 2 h of etching with 1 h of the interval, while Sample 2 is subjected to single-step 3 h of HF vapor etch. (a) Sample 1, i) unreleased sensor before stencil lithography, ii) after stencil lithography, iii) after 1 h of HF vapor etch, iv) After 2 h (1 + 1) of etching. (b) Sample 2 implemented with stencil lithography, i) unreleased sensor before stencil lithography, ii) after stencil lithography, iii) after 3 h of HF vapor etch release. No HF vapor etch damage is observed to Si NWs undergoing release after stencil lithography. (The scale bars are 10 μm.)

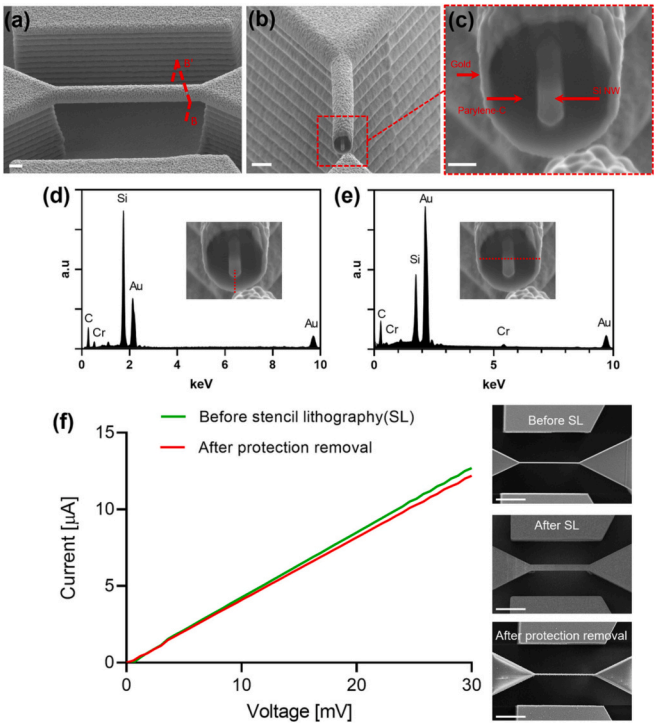


Fig. 5. Investigation of the Si NW cross section through focused ion beam (FIB) milling of NW after the stencil lithography. (a) Tilted image of the NW after stencil lithography, BB' implies the location of FIB milling (Scale bar 1 μm). (b) 90° rotated image of NW cross-section after FIB milling (Scale bar 1 μm). (c) Close-up of the NW cross section, showing the Si NW core surrounded by the dark parylene and the bright gold protective layers on all sides (Scale bar 200 nm). Gold coating thickness on NW sidewalls and bottom is around 75 nm, while the top NW surface has a 95-nm gold coating. (d-e) Validation of the presence of protective coating through energy dispersive spectroscopy X-ray spectroscopy (EDS) measurement via line plot spectra over the cross-section region. (f) SEM and electrical characterization for successful removal of the parylene and the protective metal after stencil lithography (Scale bar 5 μm). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

fabrication process flow, Si NW is conformally coated with parylene, followed by protective layer of gold (~100 nm) via stencil lithography. Chromium is used as an adhesion layer (~5 nm) in between. Hence, removal of all protective layers should involve sequential etching of gold, chromium, and parylene. A 2.5-min etching via Potassium iodide-based gold etchant (Sigma Aldrich) within a 1:1 DI water solution is used to remove gold. This is followed by a 1-min chromium wet etching (Technic) with the same dilution. After removal of the gold and chromium, sample is immersed into IPA and dried. Exposed parylene is later removed via O_2 plasma etching (Sentech Etchlab 200). Fig. 5(f) shows a Si NW coated with protective coating via stencil lithography, followed by successful removal of the protective coating after stencil lithography. Right panel shows the SEM micrographs of the Si NW before the stencil lithography, after protective coating via stencil lithography, and after the removal of protective coating, respectively, from top to bottom. SEM micrographs imply selective removal of the protective coating around Si NW without any geometrical damage. Moreover, the selective removal of the protective layers is further verified by electrical characterization through probe I-V measurements. Fig. 5(f), left panel, shows the electrical response of the Si NW before stencil lithography (green curve) and after removal of protection layer coated via stencil lithography (red curve). Electrical response of Si NW after protective coating removal follows a linear voltage-current relation, with electrical resistance roughly the same as before stencil lithography. Additionally, since electrical resistance is function of Si NW geometry as well, no degradation in electrical resistance further substantiate that no geometrical damage occurs to Si NW. Hence, both geometrical and electrical characterization verify selective removal of protective coatings around Si NW without any significant performance degradation.

Fabrication via stencil lithography offers significant advantages as the stencil can be re-used multiple times [19,20]. However, stencil contamination resulting from adhesives, stencil-sensor contact-induced membrane damage and the membrane clogging are the leading factors determining the maximum number of cycles a stencil mask can be used. In the current work, to avoid any adhesive or sensor-induced contamination, stencil is washed with acetone, IPA, and DI water to remove contamination after each stencil lithography cycle. Moreover, stencil-substrate mechanical contact-induced damage is avoided by the use of a 90-μm tape both as an adhesive and a spacer. Moreover, stencil clogging is not a significant factor as the deposited metal thickness (100 nm) is more than two orders of magnitude smaller than the stencil membrane width. Therefore the stencil can be re-used multiple times before it is cleaned for removing material accumulation on the stencil membrane. This cleaning procedure can be carried out multiple times as already demonstrated elsewhere [19,20]. In the current work, selective gold removal is achieved again in a 1:1 solution of gold etchant (Sigma Aldrich)) and DI water.

In the broader term, the developed technology enables the independent geometrical design of MEMS shuttle and Si NW by providing access to the desired feature on a multiscale device architecture for localized surface modification in a resistless manner. This has implications for localized surface functionalization of transduction structures for chemical or biological sensing applications. In current developed technological process, parylene-C was added as an insulating layer to prevent electrical contact between metal and Si NW for specific device applications. However, any material can be directly coated via stencil lithography on NW to take benefit of the maximized surface-to-volume ratio of the Si NWs for wide-range gas sensing [21,22] or biomedical applications [23,24].

4. Conclusion

Damaged caused by prolonged HF vapor etching to Si NW during the sensor release process poses a limitation for monolithic integration of Si NW with thick MEMS structures. A stencil lithography-based technology is developed that provides access for localized surface modification to Si NW on the sensor and coats a protective layer around Si NW for protection against HF vapor etching during prolonged release. The proposed technology was developed after calibrating individual process steps and implemented on a Si NW-based sensor to coat a layer of protective metal around NW. The sensor was subjected to a prolonged HF release process after technology implementation, and no damage was detected to the NWs after the prolonged release process. Therefore, the proposed technology seems promising for the independent integration of Si NWs with thick MEMS structures with an order of magnitude geometrical difference. Besides, the developed technology offers the potential for enhancing existing sensors' performance through its option to locally coat and modify Si NW surfaces for wide-ranging consumer applications.

Declaration of Competing Interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests:

Basit Ali reports financial support was provided by Scientific and Technological Research Council of Turkey.

Data availability

Data will be made available on request.

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