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Scalable Low-Power Skyrmionic Logic Gate Library

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Magnetic skyrmions, despite being promising ultra-low energy information carriers with wide bandwidth and nonvolatility, are not used for any universal scalable logic system. Here, a detailed understanding of skyrmion motion in nanowires under different geometries and drive conditions is established. Then, these insights are used to introduce a general Boolean-universal gate block system with components, emulation, and simulation algorithms. The resulting system can collectively form a scalable, cascadable, and universal skyrmion logic system and produce arbitrary logic designs. The NOR, AND, OR, NAND, XNOR, and FULL ADDER gates are provided here as example demonstrations of the system. The toolkit lays the foundation for bridging the gap between theoretical exploration and practical implementation of skyrmion-based computing. The skyrmion block components may help reduce energy consumption per logic operation after eliminating Joule heating. The insights and designs may help skyrmions be used in state-of-the-art electronic design automation.

1. Introduction

The anticipation of the breakdown of Moore's law due to quantum effects such as leakage current has prompted a more intensive search for alternative technologies to replace the complementary metal oxide semiconductors (CMOS)[1,2] Magnetic textures and particularly magnetic skyrmions, have gained a lot of attention as a potential solution since 2000s[3] and more so after their experimental confirmation in 2009 using small angle neutron scattering (SANS)[4] and Lorentz Transmission Electron Microscopy (LTEM).[5] Skyrmions are nanometric magnetic textures,[6] non-volatile at room temperature,[7] and can reach high speeds.[8] The Dzyaloshinskii–Moriya interaction (DMI) is crucial for the stabilization of skyrmions.[9] Magnetic skyrmions might offer control with several orders of magnitude lower power consumption than state-of-the-art transistors, non-volatility, ultra-high density, room temperature operation with wide bandwidth, nonlinear activation, and learning functionalities.[10] Hence, understanding the current-driven behavior of skyrmions in nanowire magnetic tracks and harnessing their merits are crucial for complementing CMOS and emerging new demands of artificial intelligence applications on nanoelectronics.

Understanding skyrmion motion, generation, and propagation dynamics within nanowires is essential for developing any skyrmion device application. An early proposal for current-induced skyrmion generation dates back to 2012.[11] The same year witnessed the experimental observation for the skyrmion motion in FeGe nano-layers for currents below 100 A cm^{-2}.[12] The skyrmion motion was experimentally observed in 2015[13] and 2017[14] for Co layers and 2017 for $Co_8Zn_9Mn_3$ layers.[15] The experimental observation of skyrmion generation and dynamics for simple geometries is essential but the modeling studies are crucial for uncovering the potentials of the skyrmionics field. Among these studies are the skyrmion motion in notched geometries,[16] skyrmion generation by constrictions,[17] skyrmion generation by local heating,[18] and DC current generation of periodic skyrmions.[19] The reversible conversion between skyrmions and magnetic domains,[20] and the role of constrictions in the skyrmion generation from domains[21,22] have also been studied. These demonstrations help validate and strengthen the place of skyrmions as reliable data signal carriers in modern logic schemes.

A key issue that prevented skyrmions from being used in applications was identified as the strong dependence or even hindrance of skyrmion motion in nanowires and constricted geometries due to their polycrystallinity or slight deviations of saturation magnetization and anisotropy. Besides, skyrmion Hall effect has also been identified as a major issue that might prevent scalable nanowire-based skyrmion devices.[23] These issues highlight that there is significant room for further understanding of materials characteristics and skyrmion devices.

For device applications, skyrmion logic proposals for AND, OR, and DUPLICATOR gates,[24] skyrmion gating by current injected DW,[25] and a similar MAJORITY gate[26] are among the first endeavors to produce skyrmion logic by leveraging the interaction between magnetic configurations. The use of Voltage Controlled Perpendicular Magnetic Anisotropy (VCMA)

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to control the skyrmion motion has been suggested in some studies.[27,28] The combination of the VCMA and Skyrmion Hall Effect (SKHE) for reconfigurable skyrmion logic has also been proposed.[29–31] Despite these diverse sets of skyrmion logic studies, a scalable systematic approach is missing. Some studies require spin-to-charge interconversion steps, which are typically highly inefficient.[26,27,31] This issue severely inhibits the scalability and cascadability of the systems. Some studies such as ref. [24] are non-universal in the Boolean logic domain. Some other studies are based on SKHE.[25,32] SKHE-dependence narrows the material parameter tolerance window and synchronization of different skyrmions in different nanowire channels. In general, the sharp synchronization requirement of the studies like refs. [24, 25, 31, 32] limits their scalability. Moreover, none of the existing studies in the literature have proposed a general scalable geometry. A reusable and robust skyrmionic logic gate system must use a single type of data signal such as only skyrmions but not additional current pulses that carry information. They must also have cascadable geometry, use the remanent properties of skyrmions for nonvolatility, and have a wider window for skyrmion signal synchronization.

Time domain scaling of the operations and skyrmion logic gates and blocks is strongly dependent on the magnitude of the magnetic domain stability that depends on effective anisotropy, their gradients, and the total magnetic energy landscape gradients. In this study, because we focus on minimizing the total energy consumption of logic operations, their gradients are also lower than some of the earlier skyrmion logic gate studies.[24] By using stronger field gradients, such as thermal field gradients[33] or fs laser pulses,[34] we and other researchers have shown the possibility of faster control of skyrmions and magnetization processes.

Scalability can bear several meanings. In this study, scalability refers to the ability to construct larger logic circuits by maintaining all geometric and operational properties of the blocks constant and connecting them like Lego pieces. Here, scalability does not pertain to the geometric enlarging or shrinking of a block. Our goal is to sustain the narrowest channels feasible to maximize the density of the logic circuit and to minimize both Joule heating and the magnetic energy costs of logic operations to approach thermodynamic limits such as the Landauer limit, which is ($k_B T \ln(2)$).

Here, we establish a detailed understanding of current-driven skyrmion motion in nanowires with different constriction geometries and demagnetization fields, and current densities. We use this understanding to solve the scalability problem by suggesting a system-level approach for skyrmion logic. This system-level approach consists of the general gate geometry, components, emulation scheme, emulation software, and automatic simulation software. The proposed system is scalable, cascadable, and Boolean universal. The emulator software can be accessed online.[35]

2. Results

2.1. Universal Logic Gates Built from Inverter Block

The introduction of the skyrmion inverter gate and the cascaded operation of two inverter gates[36] opens the possibility for a skyrmionic logic system By considering the probing skyrmion in ref. [36] as a signal that carries information, we establish the inverter functionality with this universal Boolean gate. The Boolean equation describing the operation of this inverter gate is:

$$z = \bar{x}\, y, \tag{1}$$

where x is the incoming skyrmion from the bottom channel, y is the incoming skyrmion from the left channel, and z is the output skyrmion at the output channel shown on the right-hand side. Concatenating two inverter gates horizontally similar to **Figure 1a** with a skyrmion entering from left yields:

$$o = \bar{u}\, z = \bar{u}(\bar{x}1) = \bar{u}\,\bar{x} = \overline{u + x}. \tag{2}$$

Equation (2) describes a NOR gate that is a universal Boolean gate. Since inverter gates are the sole constituents of this NOR gate, this equation confirms again that the inverter gate in our formulation can be used as a universal gate. This opens the possibility of a scalable system with inverter blocks. We expand the system here from the simplest structure of two block gates.

2.2. Two Block Gates

In this section and next sections, we combine inverter gates to achieve more complex gates. The work cycle of the inverter gate has three stages:

1) The Initialization Stage: In this stage, the spin-polarized current fills the vertical track of the device with a magnetic domain if a skyrmion is present in the vertical input.
2) The Transfer/Blocking Stage: During this stage, the spin-polarized current flows through the horizontal track and pushes any existing skyrmion in this track.
3) The Clearance Stage: In the final stage, both the domain in the vertical track and any remaining skyrmion in the horizontal track are cleared at the end of each work cycle of the inverter block. This is achieved by injecting the spin-polarized current into the vertical track as well as the side notches around the vertical track.

When combining the inverter gates to achieve more complex gates, each work cycle is repeated for each inverter gate.

Figure 1 shows NOR and AND gates, the most straightforward gates that can be constructed with a combination of inverter gates. Figure 1a shows the NOR gate of Equation (2), where x is the input1 and u is the input2. The first row shows the case where input1 is logic high (or skyrmion present). The existence of a skyrmion in any vertical inputs stops the horizontally moving skyrmion from left to right. Since the output of the gate is located at the right end, after the work cycle of the gate finishes (13.7 ns), there is no skyrmion at the output location (logic low). Thus, the output of the NOR gate with a single logic input high is zero.

On the other hand, if none of the inputs is logic high (no skyrmion exists at the inputs), as shown in the second row of Figure 1a, the horizontal skyrmion moves to the right side

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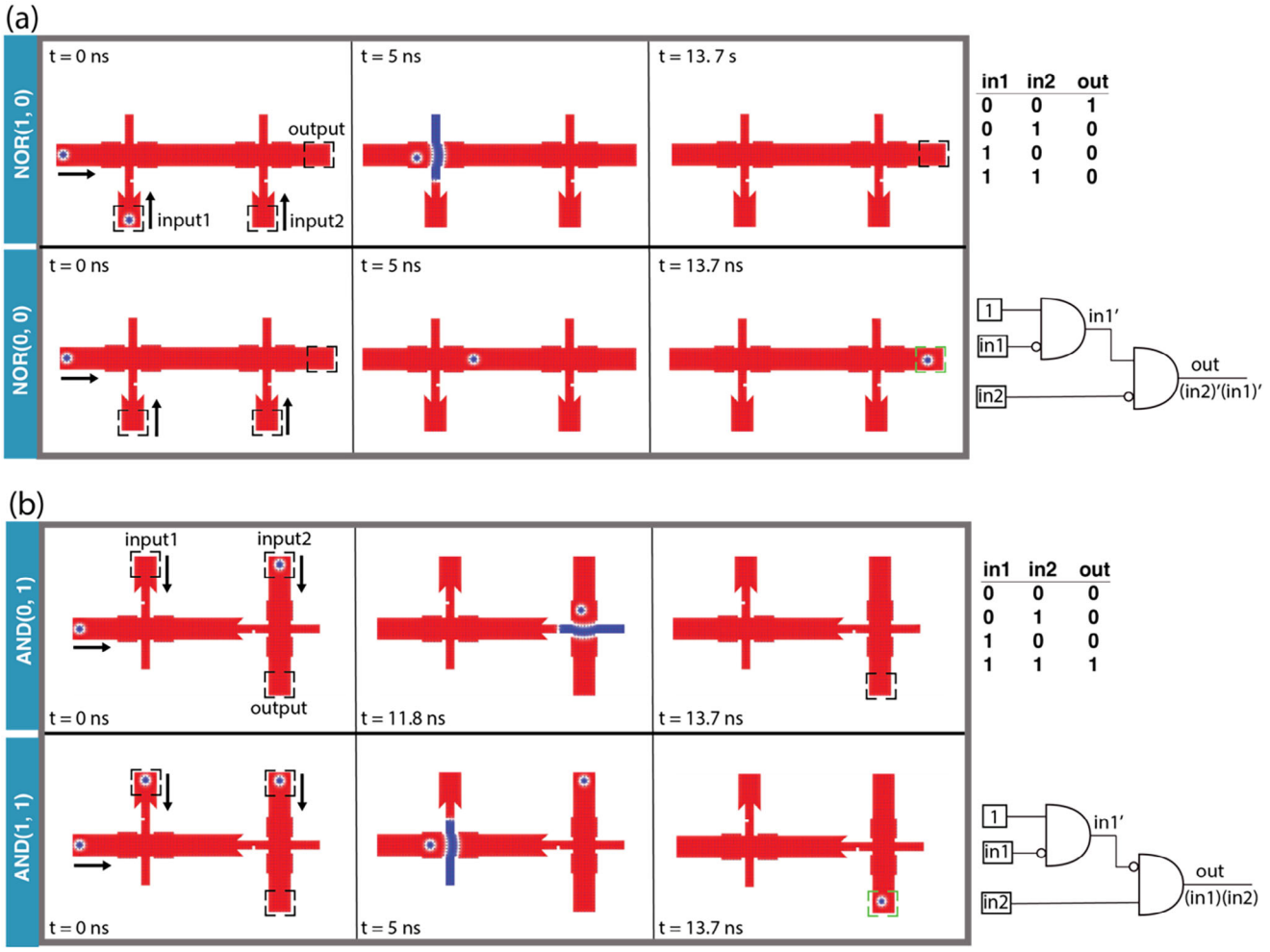


Figure 1. Two-block cascaded gates: NOR and AND. a) The NOR gate consists of cascading two inverter gates where the output of the first one is connected to the non-inverted input of the second one. b) The AND gate is a two-block gate produced by connecting the output of the first inverter to the inverted input of the second inverter.

without any hindrance. This results in a skyrmion at the output location (logic high output). The output channel (right side) of Figure 1a shows the truth table and the Boolean circuit equivalent representations of the skyrmion NOR gate.

Changing the configuration of the two inverter gates in Figure 1a into Figure 1b by flipping and rotating the right inverter block produces an AND gate. The constant logic high still exists in the horizontal channel. The output will be 1 if the skyrmion in input2 can move to the output location. Thus, if input2 is 0, the output will be 0 regardless of input1. If the input1 1/0, the skyrmion in the horizontal channel stops the skyrmion in the input2 track from moving to the output location, and the output is 0. This situation is shown in the first row of Figure 1b.

On the other hand, if input1 and input2 are 1, input1 stops the horizontal skyrmion from reaching the second inverter. In this case, the skyrmion in the input2 moves to the output location without disturbance. This situation is depicted in the second row of the snapshots in Figure 1b. The truth table and circuit representations of AND gate have been shown on the right-hand side of the spin density profiles of the logic gates in Figure 1b. Demonstration videos of the logic gates are provided online.[37]

2.3. Three Block Gates

Since an OR gate is a NOR gate with an inverted output and a NAND gate is an AND gate with an inverted output, adding an inverter to the output of the gates in Figure 1a,b results in OR and NAND gates, respectively. **Figure 2**a shows the NAND gate structure. The NAND gate is produced by adding an inverter at the output of an AND gate. The left column of the NAND figure table shows the case where the output of the NAND gate is 1, and the right column shows the case where the output of the NAND gate is 0. Figure 2b shows the OR gate. The first two rows of **Figure 3**b show the OR gate where both inputs are 0, and thus the output is 0. The third and fourth rows demonstrate the situation where input1 is 1. In this case, the output of the inverted NOR gate is 0, which results in the output of the OR gate being 1. The bottom section of Figure 2 shows the truth table and circuit schematics equivalent to the NAND and OR gates.

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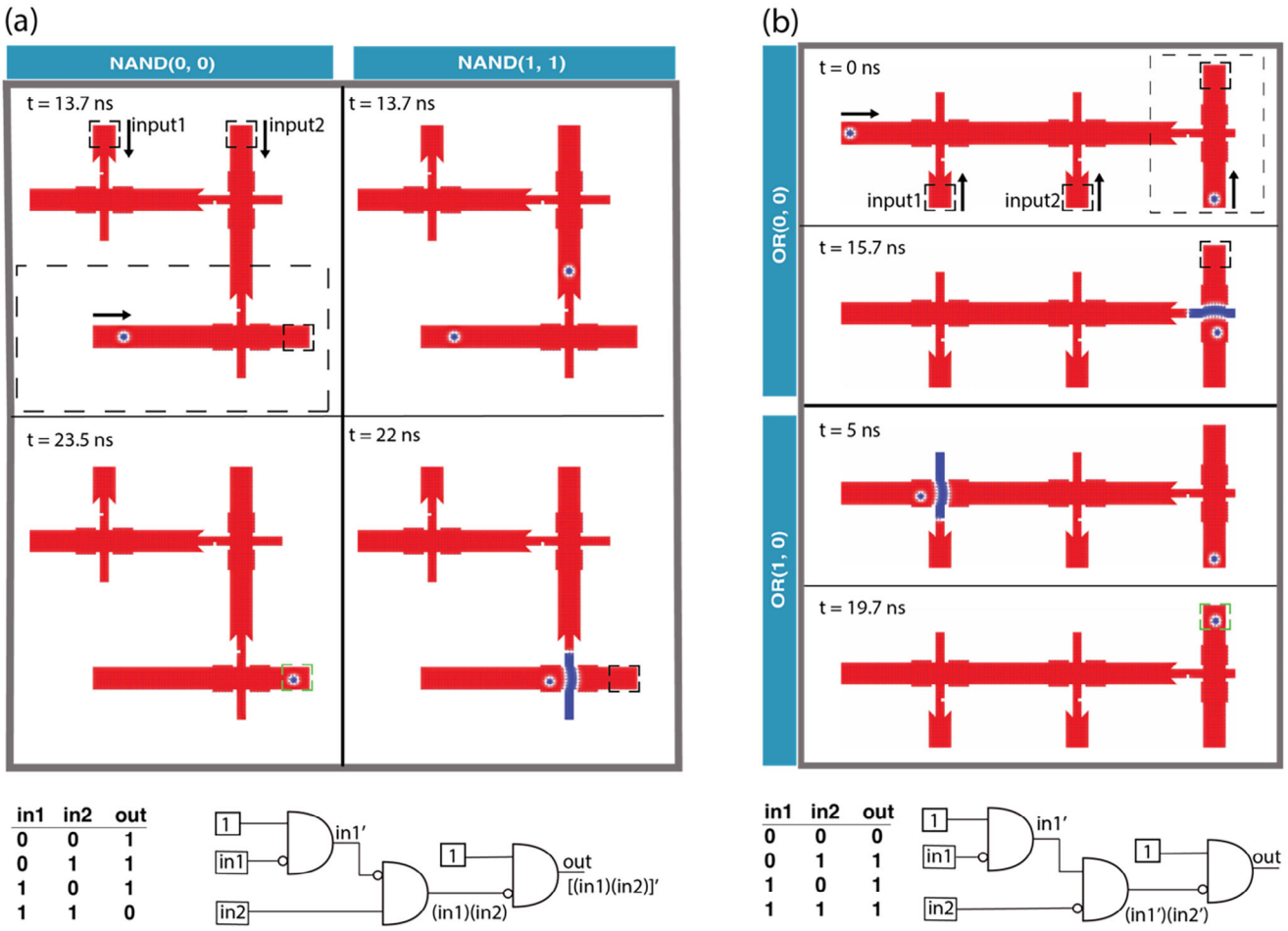


Figure 2. Three-block cascaded gates: NAND and OR. a) The NAND gate is made by adding an inverter to the output of the AND gate. b) The OR gate has been constructed by adding an inverter to the output of the NOR gate.

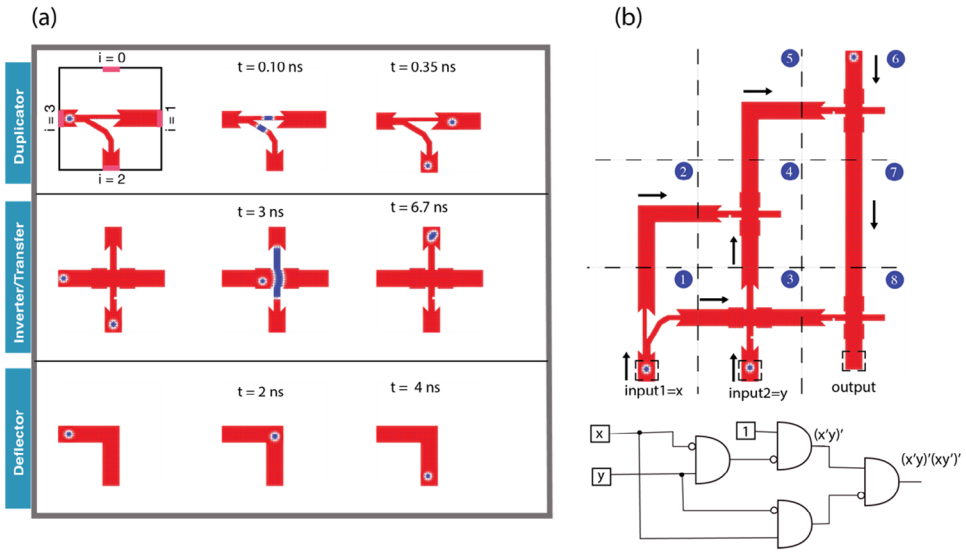


Figure 3. Blocks for arbitrary logic circuit designs. a) Three main blocks for skyrmionic logic. b) XNOR gate developed by tiling the blocks.

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2.4. Elements of the Cascadable Logic

A logic block's basic geometry is a square, featuring channels along each of its four sides. In the case of Co/Pt bilayers, these channels have a width of 50 nm, and the square sides measure 300 nm in length. Skyrmions can enter or exit the block through any of these channels. We established a naming convention for these channels, as shown in Figure 3a, using labels i_0, i_1, i_2, and i_3 to denote the top, right, bottom, and left channels, respectively.

A state equation can define the logic operation of an arbitrary gate in terms of these channels. For example, the INVERTER block's state equation is

$$\begin{cases} i_0 = 0 \\ i_1 = i_2\, i_3 \\ i_2 = 0 \\ i_3 = 0 \end{cases} \tag{3}$$

2.5. Additional Building Blocks for the Complete Logic System

2.5.1. Duplicator (DUP)

The DUP block of Figure 3a duplicates a skyrmion by breaking its topological protection by pushing it into a narrower channel. The resulting domain is then split into two domains. These domains are then pushed into the wider channels to produce two skyrmions.

The geometry of the DUP block consists of a 50 nm input track connected to the i_3 channel. This track is then connected to a 23 nm track and split into a horizontal 12 nm and a −30° 16 nm track. These tracks connect to the i_1 and i_2 channels, respectively.

The work cycle of the DUP block consists of applying a total spin-polarized current of magnitude 3×10^{12} A m^{-2} to the input track for 1 ns.

2.5.2. Inverter/Transfer (IT)

The IT block is the INVERTER block with a change in geometry by extending the vertical track to the i_0 channel by a 50 nm track. By this extension, the magnetic domain of the vertical track produces a skyrmion at the i_0 instead of being destroyed at the end of the block's work cycle. The second row of Figure 3(a) shows the IT device.

2.5.3. Deflector (DF)

The DF block moves a skyrmion from its i_3 channel to i_2 channel. The work cycle of this block consists of two stages of current application first to the vertical and then the horizontal channel each with the value of 0.3×10^{12} A m^{-2} and duration of 3 ns.

2.5.4. Block Variants

The flipped versions of these blocks are also necessary for optimal routing in the skyrmionics logic system. For example, a flipped version of the INVERTER gate with the horizontal skyrmion moving from right to left makes a right-to-left logic routing possible. The accompanying software package includes all possible variants for these blocks.[35,37]

2.5.5. Block Rotations

The external interface of logic blocks has a 90° rotational symmetry. This rotational symmetry owes to the block's square shape and the identical width and center alignment of i/o channels. This rotational degree of freedom reduces the design complexity. Because of the highly nonlinear effects in LLG and demagnetization field (Figures S1–S6, Supporting Information), there is a possibility that a rotated block might not work as expected. To test the validity of each rotation, blocks were tested for all possible rotations. Only designs with correct results for all rotations are included in the block sets. The block rotation changes the Equation (3) into a new equation where the indices of the channels are updated by Equation (4):

$$\text{new index} = \left(\text{old index} - \frac{\text{rotation}}{90}\right) \bmod 4 \tag{4}$$

2.6. Block Cascading and Interconnection

Arbitrary Boolean functions can be produced from interconnecting blocks by using block variants and rotations. Figure 3b shows an XNOR gate made from interconnecting 8 blocks. The order of operation for each block is an essential factor in properly implementing the intended logic. The numbers in the right top corner of each block of Figure 3b shows the order of operation.

The first block to run is the input1 which is a DUP block that duplicates the skyrmion into the i_3 channel of the IT block at its right-hand side and the i_2 track of its top +90° DF block. DF moves the skyrmion to the i_3 of the flipped and rotated INVERTER block at its right-hand side.

The second column's execution starts with the execution of the IT block. If the input1 is 1, there is a skyrmion at the i_3 channel and this skyrmion is stopped, and if the input2 is 1 the skyrmion in the i_2 channel of this block moves to the i_2 channel of its top block. If the input2 is 0, the skyrmion at the i_3 moves to the i_3 of its right-hand side block. In such a case, the device's output would be zero since that skyrmion blocks any downward moving skyrmion in the 3rd column, which means that if input1/input2 were 1/0, the output of the device would be 0. A similar analysis can be made for the case when input1/input2 is 0/1.

In this case, the blocks of the third column run from top to bottom. The skyrmion in the i_0 channel of the top block of the third column must always exist. In other words, the i_0 input of the top block of the third column is always 1. The analysis of the third column is straightforward. As the skyrmion moves down, if any of the i_3 inputs of the third column blocks are 1, the output will be zero. Otherwise, the output will be 1.

Alternatively, one can look at the third column of the XNOR gate as the NOR gate of the i_3 inputs of the inverter gates which are $x'y$ and xy' respectively. Thus, the output can be written as follows. This shows that:

$$o = \left(x'y + xy'\right)' \tag{5}$$

which is an XNOR gate.

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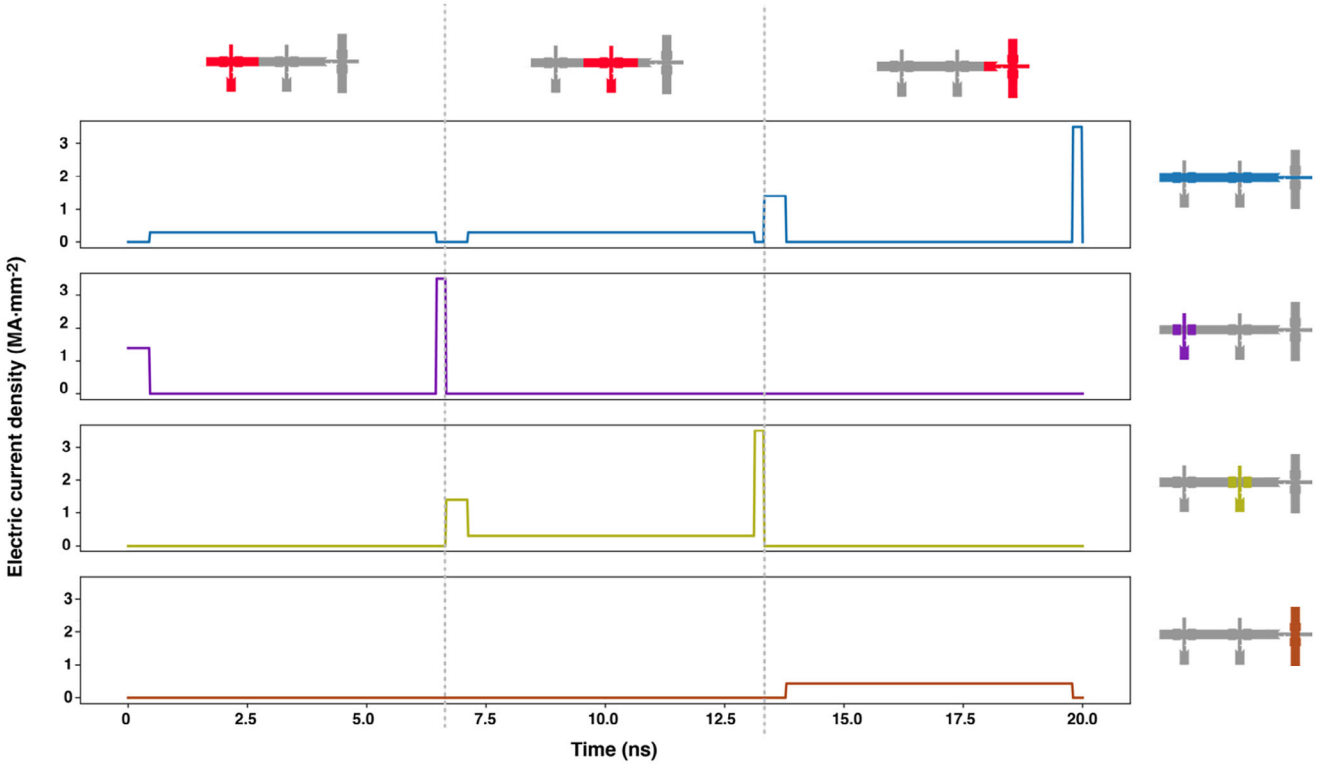


Figure 4. Track current profile for ordered execution of the OR gate. Different tracks of the OR gate with color codes corresponding to the current density. The dashed lines divide the track currents to show the active block.

2.7. Current Density Value Matching

The driving force of the skyrmionic logic system is the STT resulting from the spin-polarized current that moves in the plane of magnetic tracks. In our studies, the current density values are reported in a standard way to preserve the charge conservation principle. The current density is reported for a 100 nm wide channel and modified by a multiplier for narrower or wider channels. For example, the nominal current density of 1 A m^{-2} will be 5 A m^{-2} for a 20 nm track. The effects of different geometric aspects on the block and the logic gate characteristics have been investigated in more detail in Figures S7–S18 (Supporting Information).

Drive current densities needed by different adjacent interconnected blocks need to be compatible for a robust logic circuit operation. For example, the input current density for the vertical track of the INVERTER is 1.4×10^{12} A m^{-2}. The current density for the horizontal track of the same block is 0.3×10^{12} A m^{-2}. If we connect these blocks such that different tracks of neighboring blocks are connected, there will be current mismatch between the tracks. Case in point is the horizontal track of the AND gate of Figure 1 or the OR gate of Figure 2. This issue is solved by the application of a pulsed current. To understand this scheme, we can consider the OR gate.

The OR gate in Figure 2 is composed of three INVERTER blocks concatenated horizontally with the rightmost block rotated by −90°. These blocks constitute an integrated geometry with four interconnected tracks:

1) The horizontal track
2) The input1 vertical track
3) The input2 vertical track
4) The output track

Figure 4 shows the current profiles in these tracks. The dotted lines delineate the runtime of the three blocks. The left INVERTER block is the first to execute. The operation is started at 0 ns by applying the current of 1.4×10^{12} A m^{-2} for 0.46 ns to the input1. Then the transfer stage of this block begins, corresponding to the 0.3×10^{12} A m^{-2} pulse profile for 6 ns in the horizontal track. Then the clearance stage begins, corresponding to applying 3.5×10^{12} A m^{-2} for 0.2 ns in the vertical track of the first INVERTER and the left side notches of the INVERTER. The same pattern happens for the other two INVERTER gates.

This analysis shows that if a single gate is in its operation cycle, there is no overlap between current density values for different interconnecting tracks. Since the operation cycle of a combination of the blocks finishes after the cycle of each block has ended, a configured combination of pulses for the interconnected tracks can produce the effect of the sequential running of blocks. The complementary bias times of the pulses ensure that each block is driven without running into a high or low current density range that destabilizes skyrmions or becomes insufficient to move. We can define a combination of pulse profiles for the arbitrary order of blocks. If we cut the current profiles of the Figure 4 from

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the dashed lines, we get three pulse profiles for each block. By reordering these pulse profiles, we can reorder the blocks.

2.8. Higher Level Abstraction

The pulsed ordering shows that the modular running of the blocks with arbitrary order is possible. The presented analysis is possible for other gates such as AND, NOT, NOR, and XNOR. The track-dependent current sequence pulse profile application enables an extended system with arbitrary order execution of the blocks. Although concurrent block execution is possible for blocks with separate tracks, we will only study systems without concurrency, i.e., at most a single block is executing at every moment.

The skyrmionic logic system can be considered a block matrix. The block matrix with N rows and M columns has N×M×4 nodes. The blocks share the intermediate nodes, i.e., the $i_0/i_1/i_2/i_3$ node of each block is the $i_2/i_3/i_0/i_1$ of its neighbor top/right/bottom/left block. Thus, the number of nodes for the state of the system reduces to (M+1)×N + (N+1)×M, which equals 4×M×N only when N = M = 1 and is smaller when M>1 and/or N>1.

The value of a node is 1 if a skyrmion exists at that node and 0 otherwise. The nodes with value 1 are shown with red dots. When the block at the specific index runs, it changes the corresponding nodes to that index. Thus, the state propagation can be recorded by taking snapshots of the nodes after each block's work cycle. **Figure 5** shows such snapshots of the state propagation of the state of the XNOR gate in Figure 3.

2.9. Energy Analysis

The transfer of the energy from the electrons to the magnetization texture is non-adiabatic. Thus, to calculate the magnetic energy for the operation, we must add the energies for the parts where the input power of the system is positive. The first 4 rows of **Table 1** show the magnetic energies for different inputs of the gates per 1 nm layer thickness. The last row of Table 1 shows the Joule heating energy for a 1 nm Co and 1 nm Pt layer where the electric current passed both layers. For a more real estimate of the device energy consumption, our calculation follows the track-based current pulse application method of the Figure 4. A faster approach could be taken by adding each block's energy usage. The results of the latter would always be smaller, and the difference gets more significant as the number of the gates increases, for example, this difference for the NOR gate with two blocks is 7% (1.30×10^{-13} J, 1.21×10^{-13} J), the difference for the XNOR gate with 8 gates is 48% (6.72×10^{-13} J, 3.52×10^{-13} J)

2.10. Signal to Noise Ratio (SNR)

The signal-to-noise ratio (SNR) of the system can be defined as the ratio of expected skyrmions to the number of skyrmions detected at the output. This metric is influenced by various factors. First, in finite temperature simulations, some skyrmions are lost. However, this can be mitigated by implementing strategies such as applying external fields, utilizing thicker materials, or employing a more robust energy landscape or field gradients. Second, if a Magnetic Tunnel Junction is utilized for skyrmion readout, its Tunnel Magnetoresistance (TMR) also impacts the likelihood of missing skyrmions. Increasing the TMR of such MTJ will also increase the SNR of the system.

2.11. Full Adder

A full adder is an essential component of the arithmetic logic unit (ALU) of digital computers. The full adder has three inputs for two single-bit numbers "a", "b" which correspond to the digits of two binary numbers, and the carry-in "c_{in}" from the last operation. The full adder has two outputs for the sum and a carry-out "c_{out}" that connects to the carry-in of the next full adder. **Figure 6** shows a skyrmionic full adder made from the block system of this article. The figure shows the full adder with inputs "(a, b, c_{in}) = (1, 1, 1)". This combination of inputs is the last row of the truth table of the Figure 6iii.

Figure 6i shows the higher-level abstraction of the full adder. This full adder consists of 130 blocks in a 13 × 10 matrix of 70 logic blocks and 60 void blocks. The Φ sign shows a void block. Each block's execution order is shown on its top-left side. The logic gates of the full adder are delineated with colored boxes. The blue boxes show the two XNOR gates, the brown box shows the AND gate, the magenta box shows the AND with inverted input, and the OR gate is shown with the green box. The set of two XNOR gates make the "sum" output of the full adder, and the AND, INVERTER, and OR blocks make the "carry out" of the full adder.

Figure 6ii shows the geometry of the full adder. The white color shows the empty space, and the dark green shows the FM layer. The colored boxes are overlayed in Figure 6i,ii to show the physical extent and geometry of the gates. Figure 6iv shows a snapshot of the magnetization profile after the execution of block number 21. As shown in this figure, seven skyrmions exist at the locations in **Table 2**. The positions of these skyrmions are shown by red circles in part (i) and delineated by blue circles in part (iv) of Figure 6. Figure 6iii shows the digital logic circuit equivalent and the truth table of the full adder gate. The gates are coded with the same colors as their respective blocks for the other parts.

3. Discussion

This work focuses on eliminating some of the major bottlenecks of skyrmion logic systems, addressing limitations in existing proposals. Previous research primarily concentrated on the physics of skyrmions, resulting in non-universal and non-scalable approaches. To resolve these issues, we introduced modularization of blocks to make a skyrmion logic circuit system by creating a universal INVERTER element, routing, and fan-out components that fit into compatible geometric units, offering a comprehensive system-level perspective.

Additionally, the development of a systematic simulation and emulation process is crucial for designing and characterizing these skyrmionics devices. To facilitate this, the work introduces specialized software for systematic simulations and emulation.

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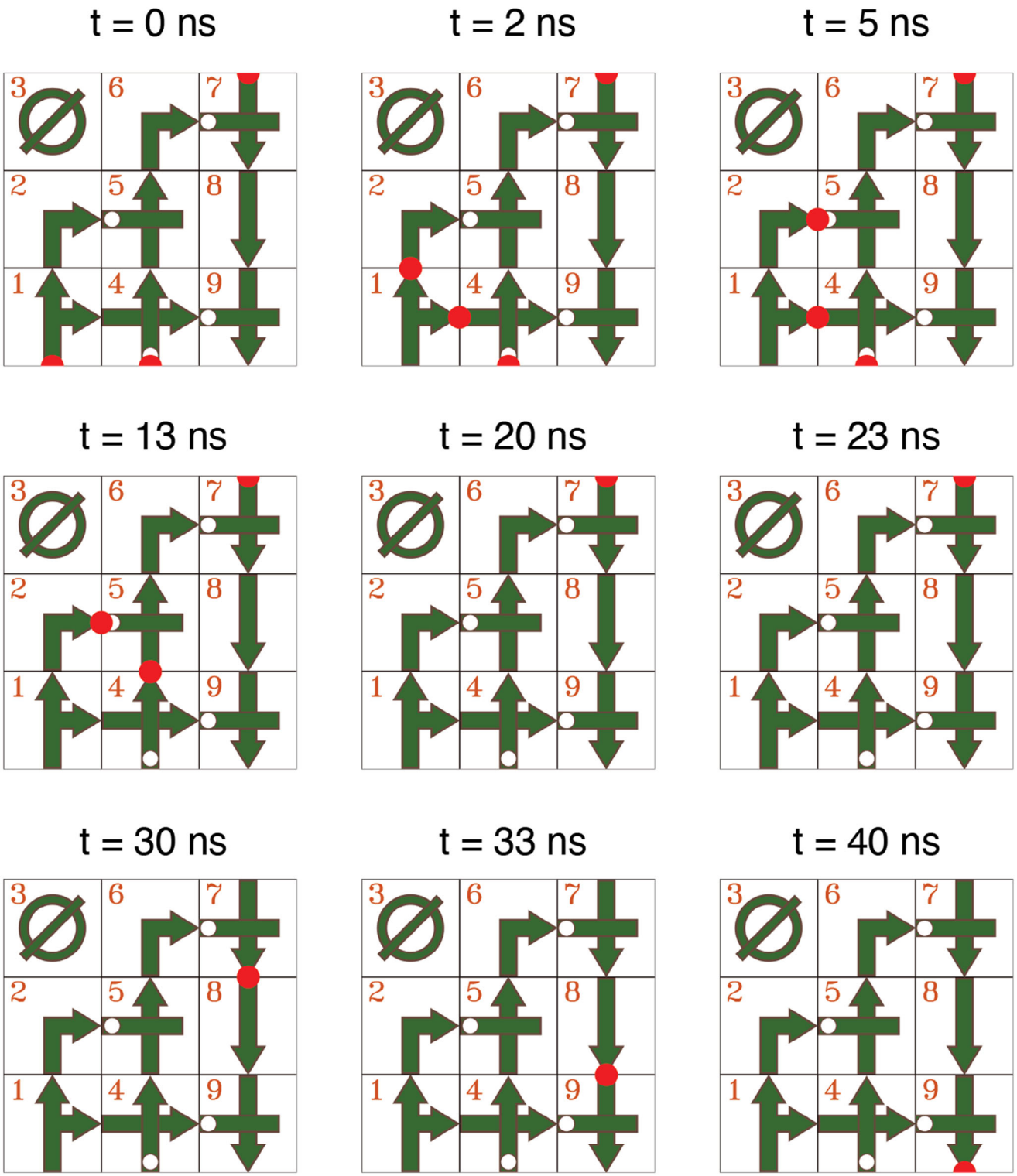


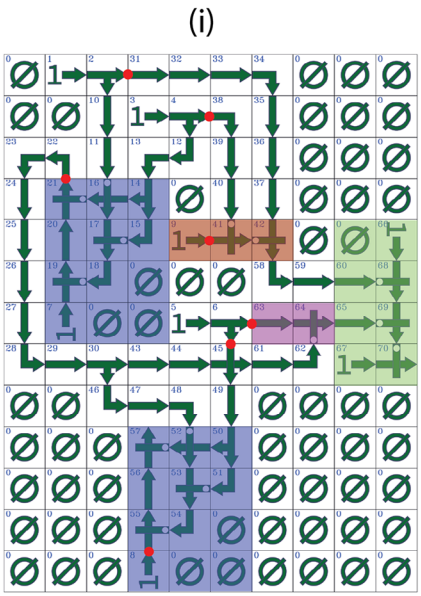
Figure 5. State propagation for the XNOR gate. The images show the snapshot of the gate at the time instance of the end of the blocks. The red circle at a node shows the existence of a skyrmion.

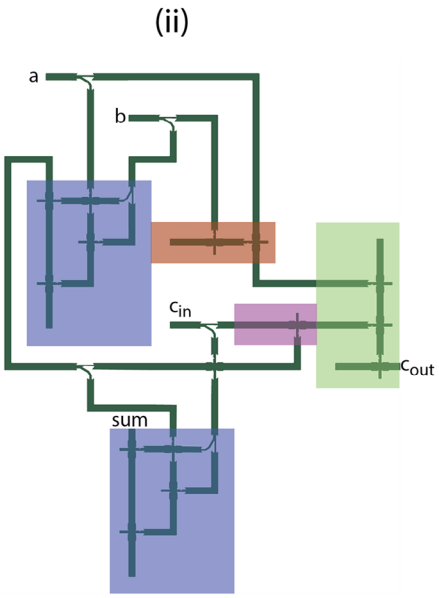
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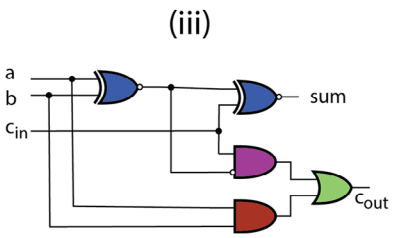
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Table 1. Magnetic and Joule energy consumptions for different inputs of the gates.

INPUTS/Type	AND E[J]	NAND E[J]	NOR E[J]	OR E[J]	XNOR E[J]
(0,0)	2.30×10^{-18}	4.82×10^{-18}	1.93×10^{-18}	4.44×10^{-18}	8.44×10^{-18}
(0,1)	2.59×10^{-18}	5.10×10^{-18}	2.59×10^{-18}	4.44×10^{-18}	9.60×10^{-18}
(1,0)	2.32×10^{-18}	4.83×10^{-18}	2.33×10^{-18}	4.45×10^{-18}	5.15×10^{-18}
(1,1)	2.59×10^{-18}	5.50×10^{-18}	2.98×10^{-18}	5.10×10^{-18}	5.92×10^{-18}
Joule Heating	1.60×10^{-13}	2.60×10^{-13}	1.30×10^{-13}	2.69×10^{-13}	6.72×10^{-13}







c_{in}	a	b	c_{out}	sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

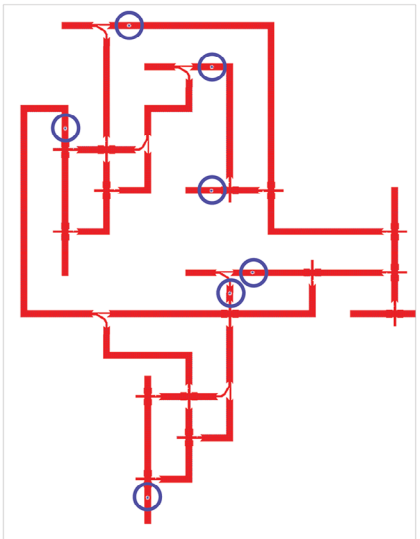


Figure 6. The full adder. i) the emulator view of the full adder. Logic gates are delineated with colored blocks; blue: XNOR, brown: AND, green: OR, magenta: INVERTER. The skyrmion positions after the execution of the block 21 are shown with red circles. ii) The physical geometry with the blocks of part (i). iii) The digital circuit representation with the same color coding and the truth table. iv) The snapshot of the magnetization profile at the end of the execution cycle of block 21. Blue circles show the position of skyrmions at this stage.

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Table 2. Skyrmions at Different Nodes after the Execution of Block 21.

Row	Column	Node
1	3	i_1
2	5	i_1
4	2	i_0
5	5	i_1
7	6	i_1
7	6	i_2
13	4	i_0

To streamline the simulation process, the work also presents a Python-based software tool for generating executable simulation scripts and files, particularly helpful as the complexity of simulations increases.

The further work of this study constitutes developing tools for VHDL/Verilog RTL schematics with skyrmion logic device layouts, necessitating an interpreter to convert HDL to the skyrmion logic blockset. Furthermore, the library of skyrmion devices and parametric studies along with further investigations into current-bias, material parameters, material noise effects, finite temperature effects, geometric variations, external field influences, and gate timing and bandwidth are beneficial.

In conclusion, this study provides a promising pathway for achieving very low energy computation by leveraging the remnant characteristics of skyrmions. However, at least four challenges must be resolved before realizing these non-volatile skyrmion logic devices. First, Joule heating must be mostly eliminated by substituting magnetic metallic layers used here with 2D magnetic insulators or semiconductors with appropriate Curie temperatures, magnetic moments, anisotropy parameters, and DMI parameters. Second, geometric pinning sites that form due to fabrication imperfections need to be eliminated on a chip scale in the fabrication process (i.e., by using a brief annealing to reflow and eliminate any undesired feature). Third, polycrystallinity and chip-scale variability of M_s, K_u, and other parameters might hamper reliable operation due to steep variations in the effective magnetic field (H_{eff}). These H_{eff} variations need to be minimized with optimal growth and fabrication. Fourth, skyrmion Hall effect might cause loss of information if it is not compensated for in magnetic materials (studied in more detail in Figures S19 and S20, Supporting Information). 2D materials with appropriate skyrmion compensation might offer the solution for minimal skyrmion drift during longitudinal transport.[23] Further materials engineering might be needed to provide a broader operation window for the logic gates.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

A.M.C. and M.C.O. have filed a patent application based on the skyrmion logic library.

Data Availability Statement

The data that support the findings of this study are available in the supplementary material of this article.

Keywords

low-power computing, non-volatile computing, scalable logic, universal skyrmionic logic

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